RECRYSTALLIZED SILICON-ON-ALUMINA AS A MONOLITHIC CIRCUIT TECHNOLOGY

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ABSTRACT

A new microwave monolithic technology based upon zone-melt recrystallization (ZMR) of silicon films on alumina substrates using a phosphosilicate glass (PSG) buffer layer is described. While initial recrystallization results confirm the difficulty of obtaining device-quality films with a thermally mismatched substrate, the planarity and viscoelastic strain relief introduced by the PSG indicates that the technology should be feasible. A surface-oriented PIN diode device structure has been developed which is compatible with the recrystallized silicon films. Results obtained with this process using single-crystal substrates demonstrate the feasibility of the device structure. The potential for high-power monolithic control circuits is discussed.

INTRODUCTION

GaAs MESFETs are recognized as viable RF control devices for applications such as switching and phase shifting in MMIC implementations. Passive two-state GaAs MESFET control devices have low bias power consumption and fast switching times and are capable of broadband operation (since the gate can be resistively isolated from the RF path). The inherent disadvantages of GaAs MESFETs in passive control applications compared to convention Si PIN diodes are twofold:

1) lower switching cutoff frequency figure-of-merit, and
2) lower power-handling capability.

This paper presents initial experimental results on a new monolithic technology to increase the power handling of MMIC control components while improving the switching cutoff figure-of-merit. Using recrystallized silicon films deposited on an alumina substrate, surface-oriented Si PIN diodes can be fabricated to obtain high-power monolithic control components. This technology eliminates the difficulty in maintaining ultra-high resistivity in bulk Si substrates after high temperature processing (1). Moreover, Si PIN diodes have higher power handling capability than monolithically compatible GaAs PIN diodes (2).

Silicon-on-alumina films have been obtained by zone melt recrystallization (ZMR) using an interface planarization/stress relief layer of phosphosilicate glass (PSG). An analysis of thin-film stress of the multi-layer structure indicates that island recrystallization should result in material with improved morphology. In parallel with the material development, a compatible silicon process was implemented, and the device structure evaluated starting with single-crystal material. In particular, a surface-oriented silicon PIN technology which features deep mesas and doped polysilicon as a diffusion source for injecting contacts has demonstrated the power-handling and switching figure-of-merit capability needed for useful devices. This new materials technology has the potential for higher-power, lower-loss MMIC control components, and it is particularly attractive for phased-array antenna modules from 1 to 5 GHz.

MATERIALS TECHNOLOGY

The ZMR technique has been extensively utilized as a means of obtaining device-quality semiconductor films on an insulating substrate. Substrate materials which have been investigated include oxidized silicon (3), fused silica and single-crystal sapphire (4) and various glasses (5). In each case, the polysilicon film which is to be recrystallized is deposited onto a highly planar surface. In this work, we used alumina (polycrystalline sapphire) since it is a well-accepted microwave substrate.

Alumina is a ceramic material formed via a high-temperature, high-pressure, tape-cast process. As such, it is a polycrystalline aggregate of randomly oriented grains and volume pore voids. It is also a brittle ceramic which does not possess a mechanism for plastic flow due to an applied stress. However, α-alumina does not undergo phase transitions at typical ZMR processing temperatures, and it is reasonably resistant to thermal shock failure. Thermal spalling characteristics are determined by the stress state of the alumina surface at a particular temperature.

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After mechanical polishing, alumina surfaces exhibit defect structures which are dominated by polishing/scoring lines and surface-grain pullouts. The polishing/scoring lines tend to be benign defects, but the surface-grain pullouts have a deleterious effect on ZMR processing since they distort surface planarity. Moreover, differential thermal expansion introduces high levels of stress and can lead to tensile failure of the polysilicon films at elevated temperature prior to recrystallization. A phosphosilicate glass (PSG) buffer layer can provide viscoelastic strain energy absorption and improve the planarity of the surface beneath the polysilicon film (6).

RECRYSTALLIZED SILICON-ON-ALUMINA FILMS

Polysilicon-on-alumina composites were fabricated utilizing the following sequential deposition procedure: chemical vapor deposition (CVD) of phosphorus-doped silicon dioxide (PSG, 8 wt% phosphorus) onto an alumina substrate, CVD of polysilicon from silane, and CVD of a silicon dioxide capping layer. The PSG was reflowed at 1000°C for forty minutes prior to the deposition of the polysilicon to planarize the alumina surface. The polysilicon was implanted with nitrogen prior to the deposition of the capping oxide for agglomeration control (6).

These composite structures were recrystallized utilizing a graphite strip heater. Fig. 1 shows a high-magnification metallograph of zone-melt-recrystallized silicon-on-alumina. It should be emphasized that the grain pull-out and polishing/scoring line defects which are visible on the alumina surface do not propagate through to the recrystallized silicon due to the planarization process. Recrystallized silicon-on-alumina films have been subjected to an etch pit analysis for determination of silicon film texture (7). The high magnification metallograph contains four square etch pits which indicate that the silicon texture is (100). Film texture was confirmed by x-ray diffractometry, with a full-width-half-maximum of less than one degree observed in the (004) diffraction peak (6).

Thus, silicon-on-alumina films can be successfully recrystallized if phosphorus is incorporated into the suboxide. The resulting phosphosilicate glass can be used to planarize the alumina substrate and to provide a high-temperature strain relief mechanism. Phosphorus doping of the recrystallized silicon film can be overcome through the choice of a suitable diffusion barrier, thereby maintaining sufficiently low I-layer doping. However, even with the PSG strain relief, full substrate recrystallization is not possible due to the difference between the thermal expansion coefficients for alumina and silicon.

A stress model was developed for the composite structure depicted in Fig. 2, assuming the strain is introduced by the differential thermal expansion between the alumina substrate and silicon film (8). At low temperatures PSG exhibits elastic behavior, and the strain is transmitted across the coherent alumina/PSG and PSG/silicon interfaces. At high temperatures, the viscosity of the PSG can be sufficiently low to result in a rate of stress relief which is much greater than the rate of stress increase introduced by the temperature ramp. Model results indicate that 500- to 1000-μm island sizes can be accommodated under normal experimental conditions. However, these results need experimental confirmation as they are strongly dependent upon the activitation energy for the PSG viscosity as well as the maximum allowable stress level in the silicon film (approximately 0.01 times Young's modulus). Based upon previous results on ZMR silicon (9), we expect that recrystallized island structures with a PSG sub-layer and a silicon nitride diffusion barrier will result in silicon films with sufficient lifetime (10 to 30 nS) for fabrication of high-performance PIN diodes.

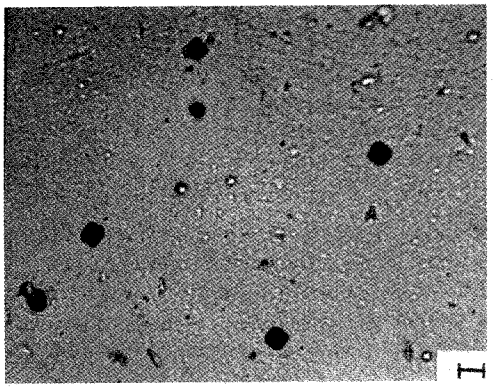

Figure 1: Metallograph of Etch Pits Depicting Silicon-on-Alumina Film Texture (the marker represents 4 μm)

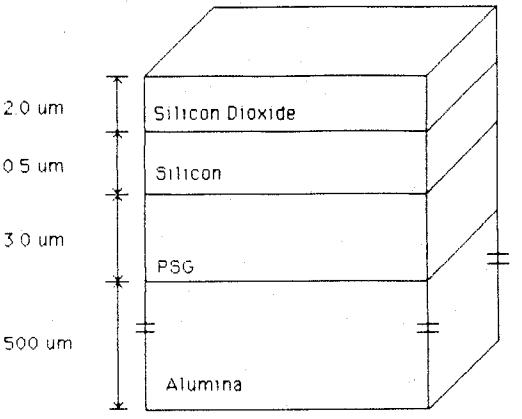

Figure 2: Cross-Sectional View of a Patterned Silicon-on-Insulator Structure used in the Stress Model [8]

LATERAL SILICON PIN DIODE FABRICATION AND PERFORMANCE

While the current recrystallized film quality is not sufficient for fabricating high-performance PIN diodes, a process has been developed in parallel which has proven successful for surface-oriented or lateral PINs. Realization of high-quality PINs in bulk Si is necessary to demonstrate the potential impact of the SOI process research. Following Battershall and Emmons (10), a sidewall injecting structure was utilized to obtain more uniform injection. A mesa structure, rather than their pocket configuration, and doped polysilicon as a diffusion source for injecting contacts were implemented, with the remaining processing steps being conventional silicon technology (11). The six-level mask process is depicted in Fig. 3.

An overall chip size of 6 mm square, selected to be compatible with the 1-inch-square alumina substrates, includes 35 probeable PIN diodes and 6 microstrip mountable PINs with I-region widths of 6, 12, 24 and 48 μm and a 150-μm periphery. The critical I-region width dimension was selected to obtain quality PIN diodes at the lower range of expected ambipolar lifetime ($\sim$ 20 nS), while allowing quantitative evaluation of this material parameter using the larger I-layer widths. One-quarter of the chip consists of various process monitoring test structures and 90°-rotated PIN diodes for studies of recrystallization anisotropy.

Using standard silicon processing procedures, the device design was evaluated starting with 10 ohm-cm (100) Si wafers. I-V data indicates that the diode ideality factor is approximately 2 over more than two decades of current. Breakdown voltages exceeded 200 V in these devices, indicating that edge breakdown is not a concern. Additional DC testing and RF evaluation of microstrip-mounted devices at 3 GHz indicate that a 3-ohm resistance is achieved with 50 mA of DC bias current. This includes an unnecessary 1 to 1.5 ohms from a parasitic series resistance due to a conservative separation between the metallization and the doped contacts near the mesa.

Based upon these results, a parasitic contact resistance of 0.25 Ω-mm (i.e. 0.25 Ω for 1-mm periphery) is achievable with this fabrication process, with a total on-resistance of 0.50 Ω-mm anticipated with device-quality ZMR silicon. This is a factor of five below GaAs MESFET control devices, with a comparable, or even lower, off-capacitance. Therefore, a factor of five increase in switching cut-off frequency is predicted compared to GaAs MESFETs, although the expected value is not as high as obtained with vertical PIN structures. In addition, the on-state current handling capability is expected to be significantly improved (not demonstrated but quite reasonable) and the off-state voltage handling has been improved by an order of magnitude compared to the GaAs MESFET. The key disadvantages of this, or other PIN control technologies, are power consumption, switching speed and component bandwidth.

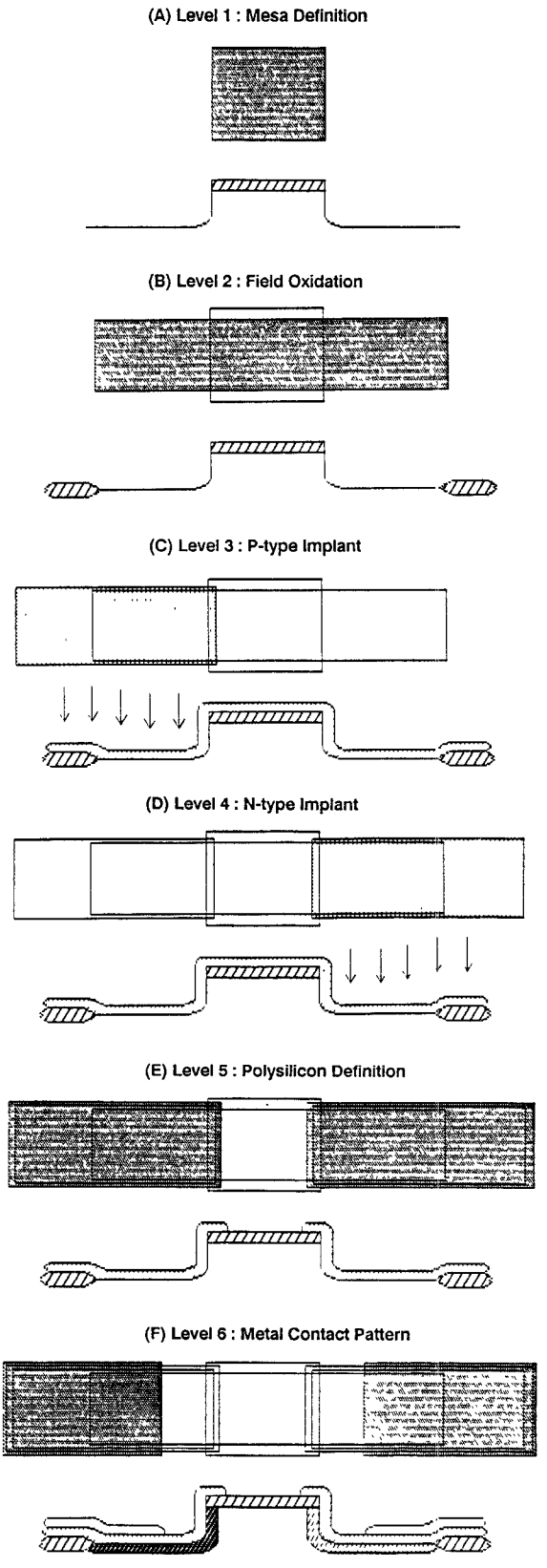

Figure 3: Mask Levels of PIN Diode Test Structure

SUMMARY

A new microwave monolithic technology based upon recrystallized silicon films on alumina substrates has been described. Initial recrystallization experiments demonstrate the effectiveness of a PSG buffer layer to improve planarity and to relieve interface stress. The technology is particularly attractive for high-power monolithic control components using surface-oriented Si PIN diodes. A compatible novel device structure using deep mesas and doped-polysilicon diffusion-source contacts has been demonstrated. The use of patterned islands, rather than continuous films, is expected to result in sufficient Si lifetime to permit implementation of this new monolithic technology, although additional technology development is needed to fully evaluate feasibility.

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